Digitally controlled phase locked loop with tracking analog-to-digital converter

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Abstract - A digitally controlled phase-locked loop (DCPLL) is described. The DCPLL has basically the same structure as a conventional analog PLL except for a tracking analog-to-digital converter (ADC). The tracking ADC generates the control signal for voltage controlled oscillator. Since the DCPLL employs neither digitally controlled oscillator nor time-to-digital converter – the key building blocks of digital PLL (DPLL), there is no need for the trade-off between jitter, power consumption and silicon area. The DCPLL was implemented in a 0.18µm CMOS process and the active area is 0.35 mm². The DCPLL consumes 59mW during the normal operation and 984µW during the power-down mode from a 1.8V supply. The DCPLL shows 16.8ps rms jitter.

I. Introduction

The phase locked loop (PLL) is widely used in digital, analog, and mixed-mode systems for various purposes such as frequency multiplication, clock synchronization, zero-delay buffering, and so on. Conventionally, the PLL is an analog circuitry where the locking information is stored as an analog signal. With the analog locking information, it is very difficult to turn off the PLL during the power-down state because the information can be lost. Therefore, the power consumption during the power-down state can be substantial. On the other hand, if the PLL is constructed with only digital circuits such as digitally controlled oscillator (DCO), time-to-digital converter (TDC) and digital control logics as shown in Fig. 1 (digital PLL : DPLL), the DPLL can be turned off during the power-down state [1]. Additional benefit of the DPLL is its easy portability to different process technologies. The jitter and locking accuracy of the DPLL depend on the time step provided by the TDC and DCO. The smaller time steps of TDC and DCO, usually the larger power consumption and silicon area.

The main requirement on the PLL of this work is power-down capability during the standby state of the system. For that purpose, it is sufficient to store the locking information of the PLL as digital code even if the PLL contains analog circuit blocks. Therefore, the PLL of this work is not a DPLL but a digitally controlled PLL (DCPLL). Neither DCO nor TDC is employed in the DCPLL. Instead, as in conventional analog PLL (APLL), voltage controlled oscillator (VCO) is used and its analog control signal is generated by a digital-to-analog converter (DAC) embedded in a tracking ADC loop. The locking information is stored as the digital input of the DAC and thus the DCPLL can be powered down during the standby state. The tracking ADC has 10-bit resolution to provide the sufficient locking accuracy and jitter performance to the DCPLL. The detailed description of the DCPLL and the experimental results are given in the following sections.

II. Digitally controlled phase locked loop with tracking analog-to-digital converter

As the conventional APLL [2-3], the proposed DCPLL shown in Fig. 2 employs a VCO, frequency divider, phase frequency detector (PFD), charge pump (CP), and loop filter. The difference from the conventional APLL is the tracking ADC which generates the control signal for the VCO. With this tracking ADC, the analog control signal at the loop filter output is converted to a digital code which enable the digital control of the loop.
The DCPLL has two feedback loops. One is the global feedback loop for the locking of the DCPLL and the other is the tracking ADC loop converting the low-pass filtered PFD/CP output to the digital code. In order for the local feedback loop, the tracking ADC loop, to have a negligible effect on the stability of the DCPLL, the bandwidth of the tracking ADC loop is designed to be much wider than that of the global feedback loop.

A. Tracking ADC

The tracking ADC shown in Fig. 3 has 10-bit resolution for sufficient locking accuracy and jitter performance. The low-pass filtered PFD/CP output is compared with the output of the DAC and the 10-bit counter is toggled until the difference between the low-pass filter PFD/CP output and the DAC output becomes smaller than the magnitude of 1-LSB.

During the power-down mode of the DCPLL, the PFD and CP are turned off and thus the loop filter output is floated. The loop filter output can therefore deviate from its original value obtained during the normal operation. When the DCPLL wakes up from the power-down mode, the tracking ADC changes the DAC input digital code because the loop filter output and the DAC output are different. That is, the DCPLL must be re-locked before the system can begin its normal operation. In order to prevent the loop filter output from floating during the power-down mode, a switch is added between the loop filter output and the DAC output as shown in Fig. 3. This switch is turned-on during the power-down mode and the loop filter output is ensured to be the same as the DAC output.

B. Digital-to-analog converter in tracking ADC

The glitch of the DAC in the tracking ADC loop plays a key role in determining the jitter of the DCPLL. To minimize the glitch, the 10-bit DAC is thermometer coded and built with the segmented structure: 9-bit with unit current cells and 1-bit with a binary scaled current cell [4]. The array of the current cells is configured as a four by five matrix.

If some mismatch between the control signal paths for the row and column switch exists, thermometer coded DAC still exhibits large glitch when another row is selected as shown in Fig. 4-(a) [5]. If the column (row) control path is faster, one less (more) row of the current cells are temporarily selected, creating large glitch. To avoid this problem, the improved decoding scheme shown in Fig. 4-(b) which has been proposed in [5] is adopted. This scheme uses different control logics for even and odd rows and limits the glitch to be less than 2-LSB even with delay mismatch between column and row control signals.

C. Comparator

Even with the input offset voltage of the comparator, the DCPLL can be locked. At the completion of the locking, of course, there would be some difference between the outputs of the loop filter and DAC. However, the offset of the comparator must still be compensated. During the power-down state, the loop filter output is forced to be the same as the DAC output to prevent the loop filter output from floating and enable fast wake-up. If the locked value of the loop filter output is different from the DAC output due to the input offset of the comparator, the DCPLL should be re-locked when the system exits from the power-down state.
As shown in Fig. 5-(a), the comparator is composed of the pre-amplifier and sense-amplifier type latch where the input offset is compensated [6]. Because the control voltage can vary in a wide range, the pre-amplifier of the comparator employs a rail-to-rail input stage to allow a wide input range as shown in Fig. 5-(b). The timing of the comparator is shown in Fig. 5-(c) where Φ1 and Φ2 are non-overlapped clocks. When Φ1 is high, the input and output nodes of the pre-amplifier are connected to the reference voltage and the offset voltages are stored on the capacitor. When Φ2 is high, the offset voltages are cancelled and only the input differential voltage is amplified. When ΦLatch is ‘LOW’, the output nodes of latch are pre-charged to VDD. When ΦLatch goes to ‘HIGH’, the latch senses the outputs of the pre-amplifier.

D. Voltage controlled oscillator

The VCO shown in Fig. 6-(a) is a fully differential ring oscillator for small sensitivity to common-mode noise. The oscillation frequency can be controlled from 350MHz to 1.3GHz as shown in Fig. 6-(b). The active VCO control voltage range is from 0.6V to 1.1V. The replica bias ensures the constant swing of the output of the VCO [7].

III. Experimental results

The DCPLL with a tracking ADC has been implemented in a 0.18µm CMOS process. A microphotograph of fabricated PLL is shown in Fig. 7. The active area of the DCPLL is 1.0mm×0.35mm. Fig. 8 shows the locking behavior of the DCPLL simulated by HSPICE. The measured reference and output clocks are shown in Fig. 9. The rms jitter of the DCPLL is measured to be 16.8ps as shown in Fig. 10. With 1.8V supply voltage, the DCPLL consumes 59mW during the normal operation and 984µW during the power-down state. The measured performance of the DCPLL is summarized in Table 1.
IV. Conclusions

A digitally controlled phase-locked loop (DCPLL) with tracking ADC has been fabricated in a 0.18µm CMOS process. The DCPLL has basically the same structure as a conventional analog PLL except for a tracking analog-to-digital converter (ADC). The tracking ADC generates the control signal for voltage controlled oscillator. The locking information is stored as the digital code and thus the DCPLL can be powered down during the standby state. Since the DCPLL employs neither digitally controlled oscillator nor time-to-digital converter – the key building blocks of digital PLL (DPLL), there is no need for the trade-off between jitter, power consumption and silicon area. The DCPLL was implemented in a 0.18µm CMOS process and occupies 0.35 mm² of on-chip area. While consuming 59mW during the normal operation at a 1.8V supply, the DCPLL shows 16.8ps rms jitter.

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References